REQUEST FOR A CORRECTED OFFICE ACTION:

The present Action states in paragraph 8 that "Claims 16-30 and 32-36 are rejected under 35 U.S.C. §103(a) as being unpatentable over DiStefano et al (Reference cited by applicant) in view of Korleski (U.S. Patent 5,545,475)."

The rejection cannot be responded to because a DiStefano et al reference is referred to only by name and eight patents to DiStefano et al have been cited by Applicant. The patent number of the DiStefano et al patent is omitted. Applicant has no way of knowing which one of the eight DiStefano et al references the Examiner intended unless a corrected action is issued identifying by patent number the intended DiStefano et al reference.

Issuance of a corrected Office Action and restarting the time for responding thereto is requested. MPEP §710.06. This request is made within one month of the mailing of the present defective Office Action and so the time should be restarted.

RESTRICTION REQUIREMENT:

Reconsideration of the restriction requirement which the Examiner has now made final is respectfully requested. Applicant elected (with traverse) the claims of Group II including claims 16-36 drawn to an interposer in the previous response.

Claims 1-15 of Group I are directed to an electronic package comprising at least one electronic device and a solderable flexible adhesive interposer having certain recited features.

Claims 16-36 of Group II are directed to a solderable flexible adhesive interposer having the same certain recited features as the solderable flexible adhesive interposer recited in claims 1-15. It is submitted that at least claim 1 of Group I and at least claim 16 of Group II require the same particulars for patentability and so restriction as between Groups I and II is improper and should be withdrawn.

The Examiner's stated reason for maintaining the restriction is that "Second, examiner has distinct (sic) 'at least two adjacent layers' which are start (sic) at two layers, one layer is not equal to two layers; therefore Group I is distinct from Group II." The reasoning is faulty and illogical. Both claim 1 of Group I and claim 16 of Group II recite the same structure, namely "at least one layer of flexible dielectric adhesive" and so both claims

of Group I and of Group II read on structures having one, two, three or more layers, i.e. structures having a plurality of layers. Thus, the Examiner's distinction is without basis in fact, and so the restriction requirement should be withdrawn.

Examination of the claims of Groups I and II in the present Application is consistent with both the extent of a proper search and with other patents, and a proper search must encompass prior art relating to interposers of one and plural layers and utilized with a wide variety of electronic devices and substrates, for the reasons set forth in the previous response.

Claims 37-51 of Group III are directed to a method for making a solderable flexible adhesive interposer having certain recited features which are similar to those of the claims of Groups I and II. The searching required for examination of all of the claims pending is not substantially greater that is examining only the claims of Group II, for example, because the references that disclose the article also in many instances also describe the method for making the article. For example, U.S. Patents 6,288,905 and 6,376,769 (issued from priority applications to the present application), both include claims directed to an article and to the method for making the article, and U.S. Patent 6,376,769 includes claims directed to an interposer, to a package including an interposer, and to a method for making the package.

Thus, examination of the claims of Groups I, II and II is consistent with PTO practice in many other applications relating to similar technology, including U.S. Patents 6,288,905 and 6,376,769, just mentioned. Other references cited in U.S. Patent 6,376,769 are similar. There is no legal or logical reason for an inconsistent result in this Application.

Accordingly, it is requested that the restriction be reconsidered and withdrawn, and that all of Applicant's claims 1-51 be examined in the present Application.

<u>OBJECTION TO THE DRAWING:</u>

The drawing is objected to because a reference character "110" is alleged to designate both substrate and flexible interposer and because "element contact 112" is not shown in Figure 1.

The objection regarding the reference character "110" is overcome by the amendment to the specification at page 6 wherein the phrase "which is a substrate" is added to clarify that

item 110 is a flexible interposer and also is a substrate, as set forth, for example, in the paragraph beginning at page 6, line 29. In other words, either term is correct and may be used for item 110 because the flexible interposer 110 serves as a substrate 110 on which chip 120 is mounted.

The drawing is amended at Figure 1 to add conductors 112 and the reference character 112 identifying the conductors connecting interconnections 124 and contacts 114 as described, for example, in the paragraph beginning at page 6, line 29. A copy of Figure 1 with the amendment indicated in red is submitted herewith.

Accordingly, the basis for the objection is removed and the objection should be withdrawn. Examiner is thanked for pointing out these informalities.

OBJECTION TO THE SPECIFICATION:

The specification is objected to regarding a designation reference at page 8 and blanks at page 10. The specification is amended to respond to the Examiner's objections and also to correct a designation " 100' " to " 100" " in the paragraph on page 8. Accordingly, the objection is overcome and should be withdrawn. Applicant thanks the Examiner for pointing out these informalities.

REJECTION UNDER 35 U.S.C. §112:

Claims 16-29 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner points out two places in each of claims 16 and 23 where the phrase "one of an electronic device and a substrate" is recited. Applicant traverses the rejection.

The phrase "one of an electronic device and a substrate" is logically and grammatically the same as saying "an electronic device or a substrate" and is accepted proper and definite claim terminology. The phraseology "one of A and B" was often utilized in place of the phrase "A or B" in the years before the Patent Office guidelines were changed to allow "or" statements in claims. Thus, claims 16-29 are not indefinite.

Withdrawal of the rejection is solicited.

PRIORITY CLAIM:

The specification was previously amended at page 1 to also include a claim to the priority of U.S. Provisional Application Serial Number 60/180,544 filed February 7, 2000, and Applicant claimed the priority thereof in the present Application. It is noted that the present Application was filed prior to the effective date of the present rule regarding priority claims. Applicant requests that the record reflect priority to Application Number 60/180,544.

CONCLUSION:

Applicant respectfully requests that the restriction be reconsidered and withdrawn, that the objections and rejection addressed herein be withdrawn, that the drawing amendment be approved, and that the Application including claims 1-51 be examined.

Applicant further requests that a corrected Office Action be issued and that the time for response be restarted.

No fee is due in this timely-filled response. Should any fee be due in consequence of this response, please charge such fee and deposit any refund to Deposit Account 04-1406.

The Examiner is requested to telephone the undersigned attorney if there is any question or if prosecution of this Application could be furthered by telephone.

Respectfully submitted,
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APPENDIX

SPECIFICATION PARAGRAPH(S) SHOWING AMENDED WORDING:

Paragraph beginning at page 6, line 29:

FIGURE 1 is a side cross-sectional schematic diagram of an exemplary embodiment of an electronic package 100 having a substrate 110 according to the present invention attached to a next-level substrate 140. Package 100 includes a flexible interposer 110 <u>which is a substrate</u> upon which an electronic device, for example, semiconductor chip 120, is attached. Contacts on the bottom face of chip 120 are directly connected to contacts 112 of interposer 110 by interconnections 124, which may be of solder or an electrically-conductive flexible adhesive. Where support for chip 120 in addition to that provided by connections 124 is desired, flexible dielectric underfill adhesive 126 is employed to fill the volume between chip 120 and interposer 110 that is not filled by flexible connections 124. Solderable contacts 114 on interposer 110 correspond to contacts 112 on the opposing surface thereof, and provide contacts for connections 134 between package 100 and conductors on next-level circuit substrate 140. Connections 134 may be conventional solder connections or electrically-conductive adhesive as in a ball grid array (BGA) package, and an underfill material is not required between package 100 and next-level substrate 140.

Paragraph beginning at page 8, line 29:

FIGURE 2 is a side cross-sectional schematic diagram of an alternative exemplary embodiment of an electronic package 100" according to the present invention attached to a next-level substrate [110] <u>140</u>. Package 100", like package 100, includes flexible interposer 110, and electronic device or chip 120 attached thereto, but with contacts on chip 120 connected to contacts 112' of interposer 110 by bond wires 125. Bond wires 124 are preferably fine gold or aluminum wires, such as are known and in widespread use in electrical devices. Contacts 112 may be formed of standard lead-frame metals, such as copper, nickel or kovar alloy, which and may also form a die-attach pedestal under chip 120 as well. Chip 120 is attached to flexible adhesive interposer 110 by a flexible or a rigid die-attach adhesive 126'. Interposer contacts 114 provide contacts for BGA solder or conductive adhesive connections 134 between package [100'] <u>100"</u> and conductors on next-level circuit substrate 140; without underfill. Lid 130 attached to interposer 110 provides mechanical protection for chip 120. An optional flexible adhesive pad 132 may be employed to provide added mechanical support and covering for chip 120, and optional metallic rim 118 may be provided for stiffening, all as described above.

Paragraph beginning at page 10, line 17:

It is also noted that where lid 130 includes a pre-applied adhesive around the

edges thereof that adhesively attach to flexible adhesive interposer 110, packages 100, 100" may be assembled in an in-line process, such as by standard pick-and-place component mounting equipment. While such lids 130 may be provided in several ways including by dispensing adhesive onto each lid or cover, or by applying an adhesive preform to each lid or cover, adhesive preform lids and covers as described in U.S. Patent No. [_____] 6,138,128 (U.S. Patent Application Serial Number 09/232,936 filed January 19, 1999) entitled "Method Of Making An Adhesive Preform Lid, As For An Electronic Device" and laminated adhesive lids and covers as described in U.S. Patent No. [_____] 6,409,859 (U.S. Patent Application Serial Number 09/337,453 filed June 21, 1999) entitled "Method Of Making A Laminated Adhesive Lid, As For An Electronic Device" which are expressly incorporated herein by reference in their entireties, are well suited to packages 100, and 100". With such low cost lids and covers and in-line processing, the cost of packages according to the present invention could be comparable to the cost of glob-top and molded encapsulation packages.

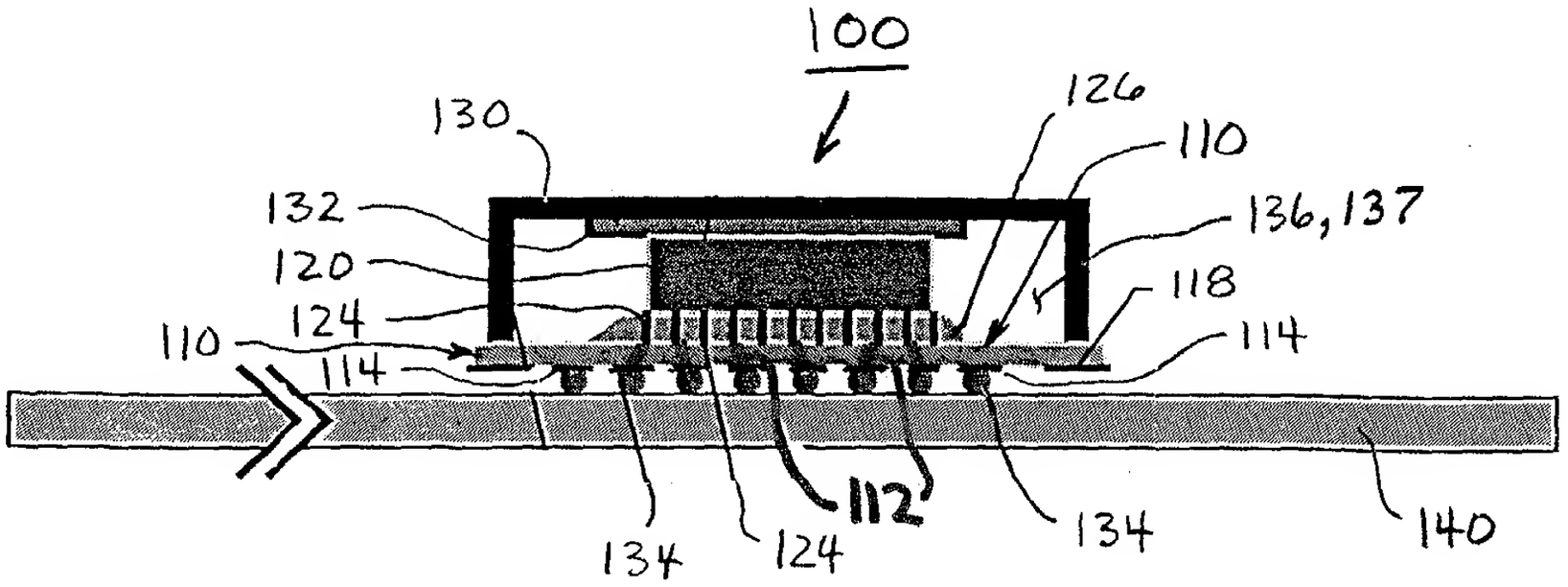

FIG. 1.

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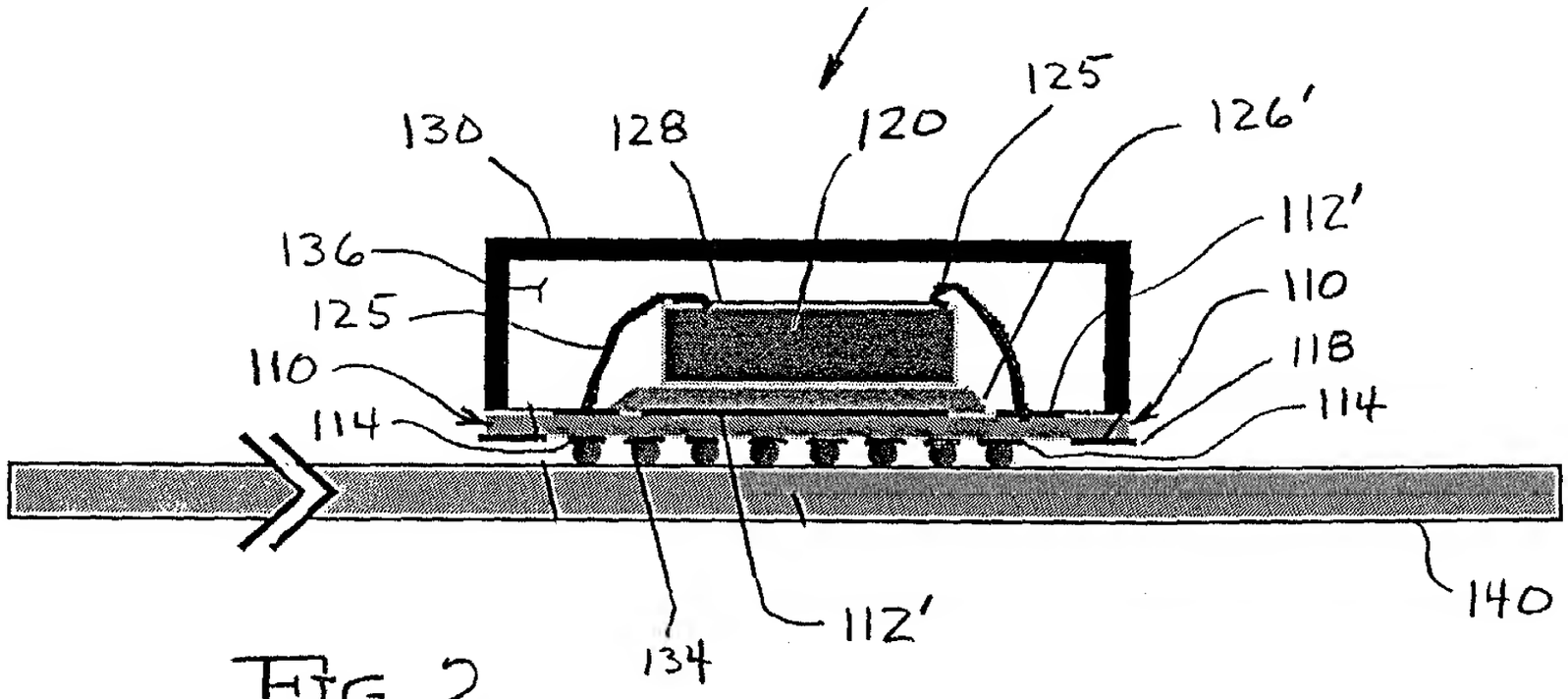

FIG. 2.

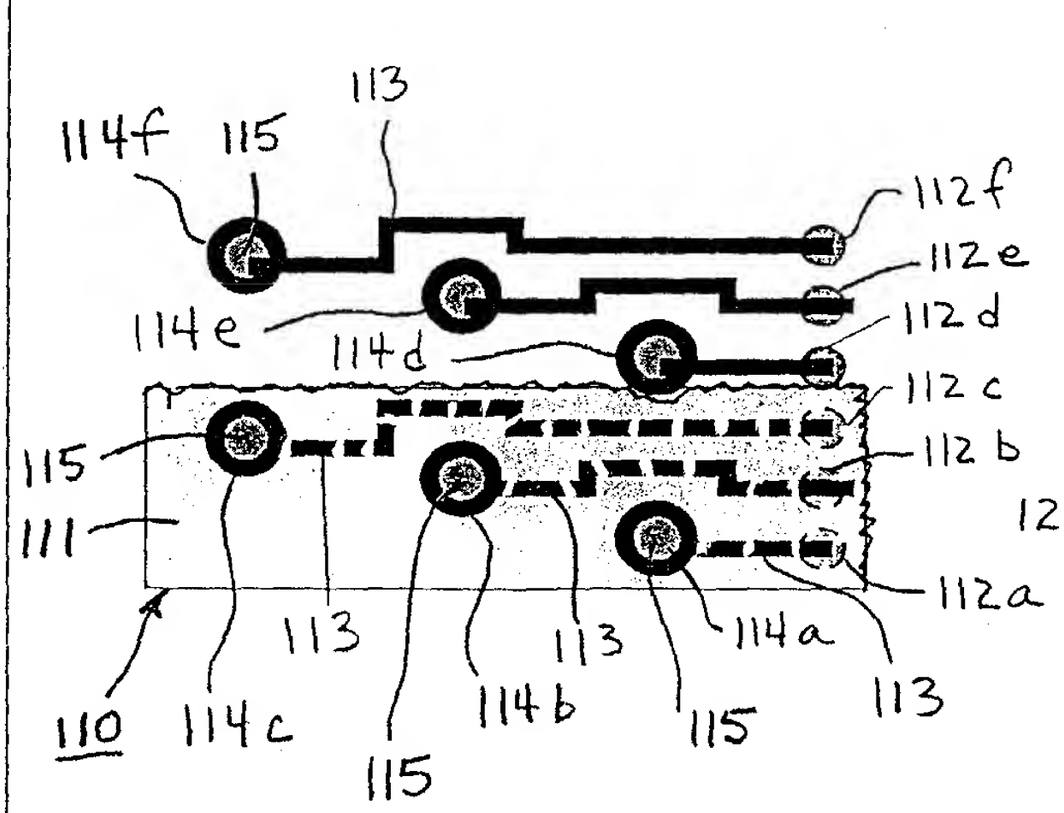

FIG. 3A.

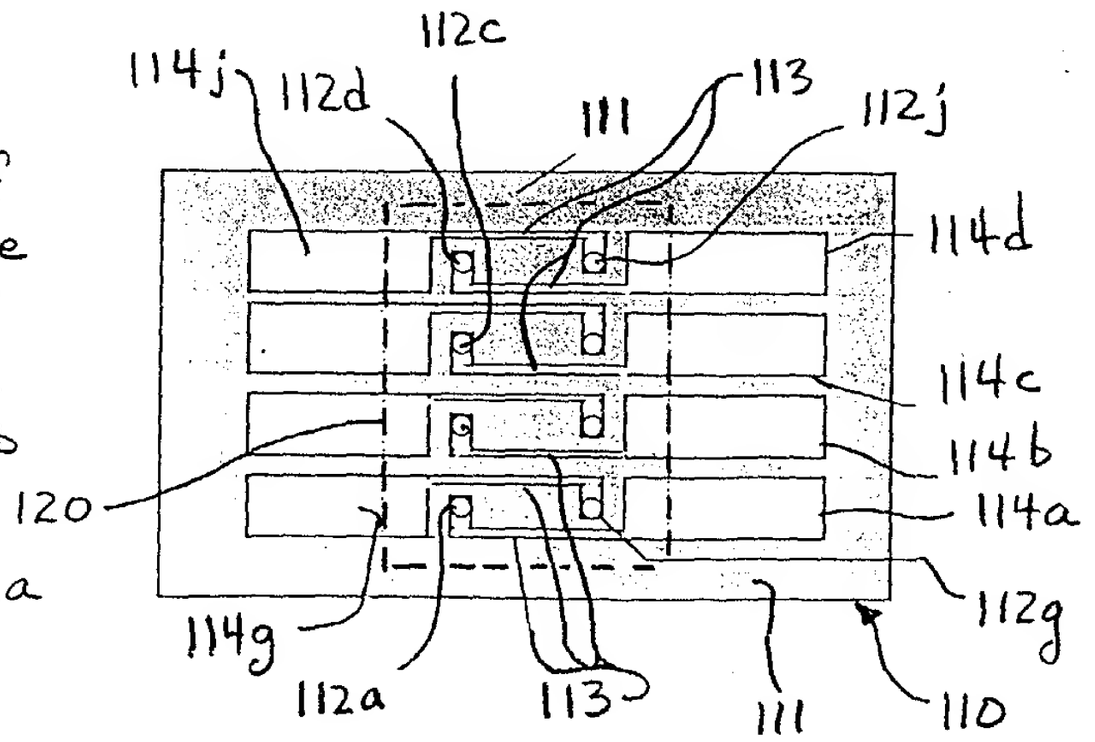

FIG. 3B.